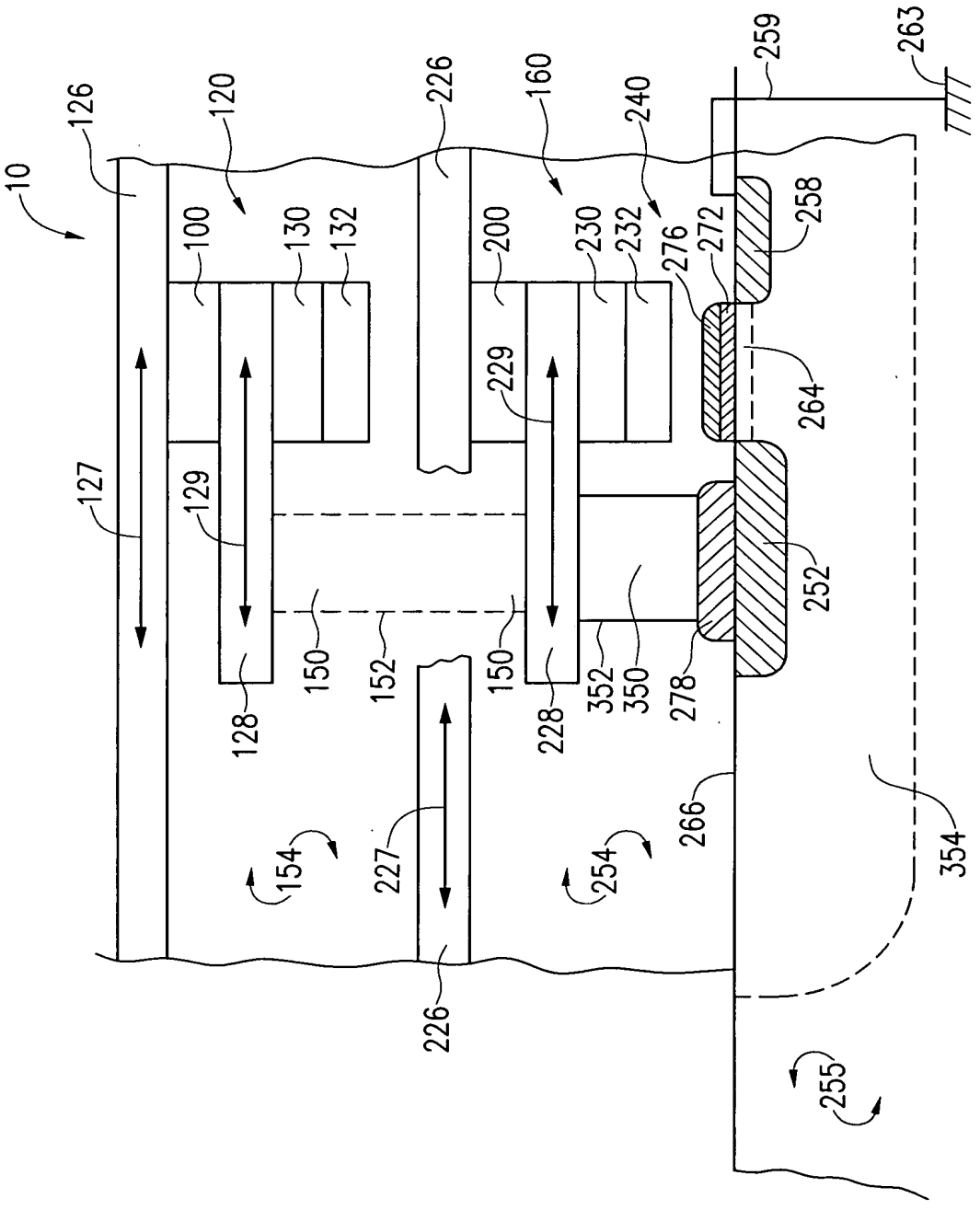

FIG. 1A

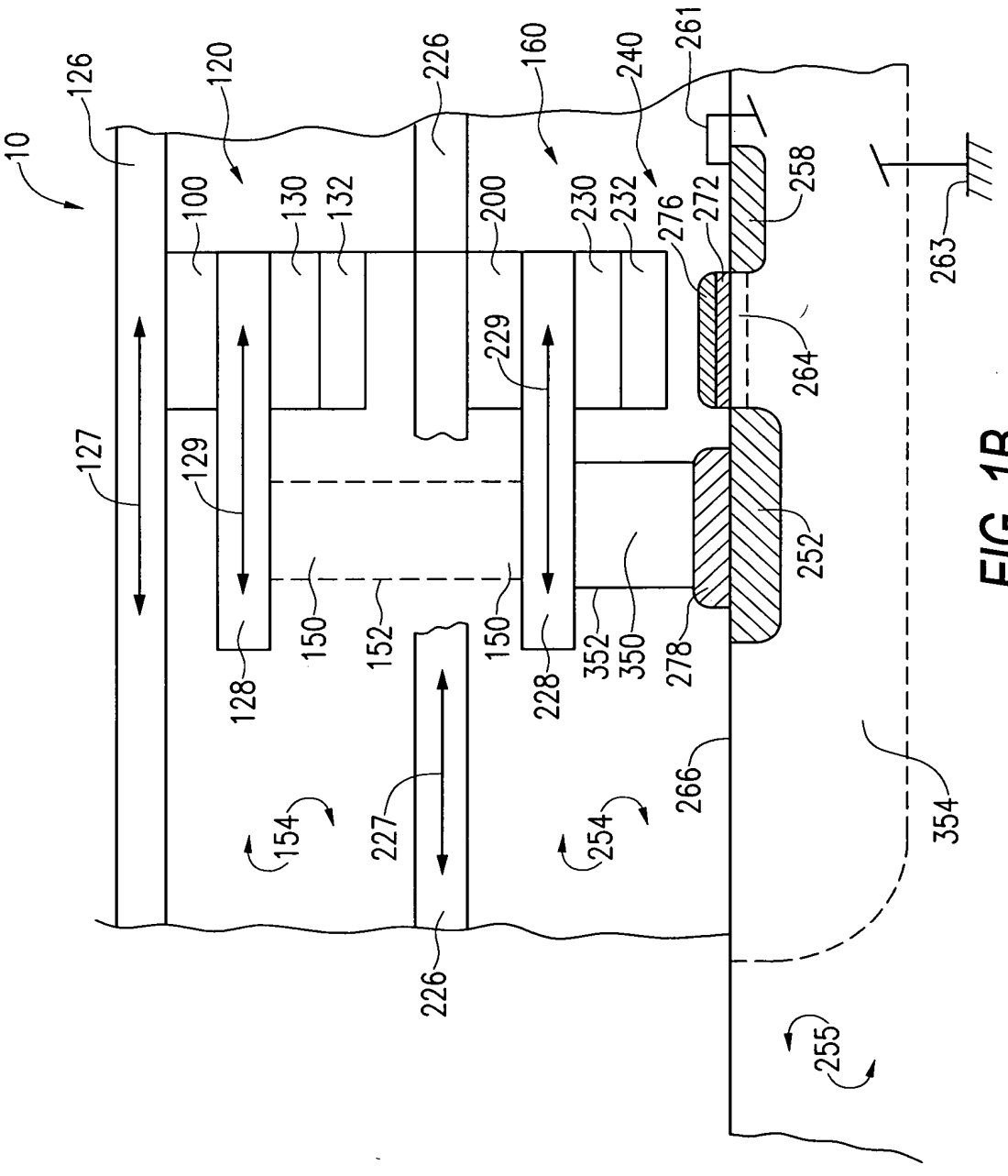
10
126
120
226
160
240
261
100
130
132
200
230
232
276
272
258
263
264
229
127
129
252
150
152
150
352
350
278
128
228
154
227
254
266
354
226
255

FIG. 1B

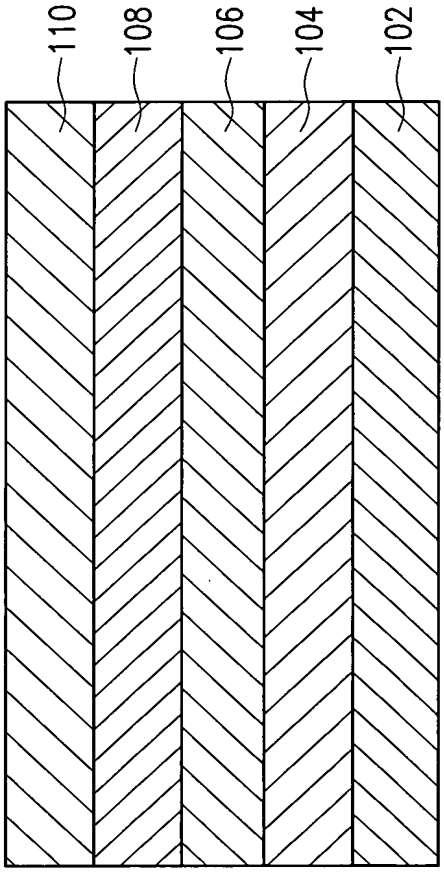

FIG. 2

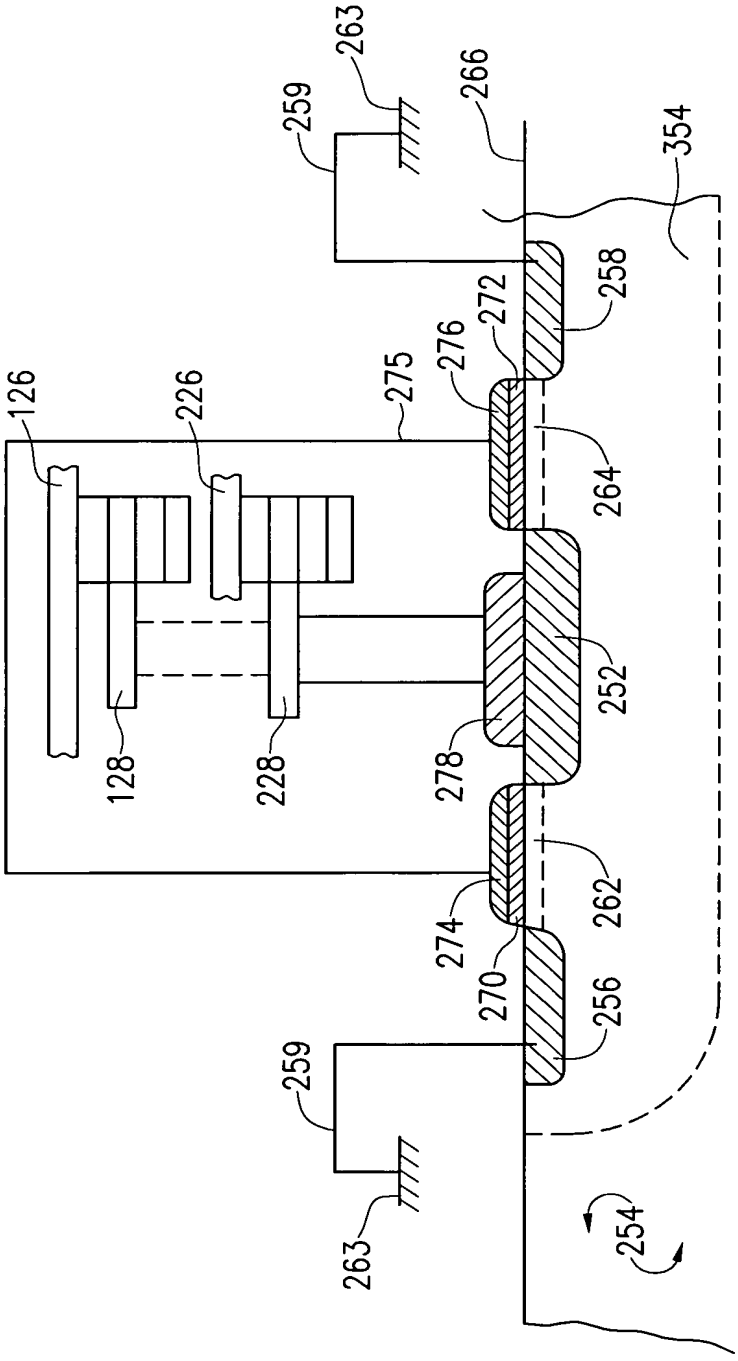
263
259
266
354
258
272
276
275
126
226
264
252
128
228
278
262
274
270
256
259
263
254

FIG. 3A

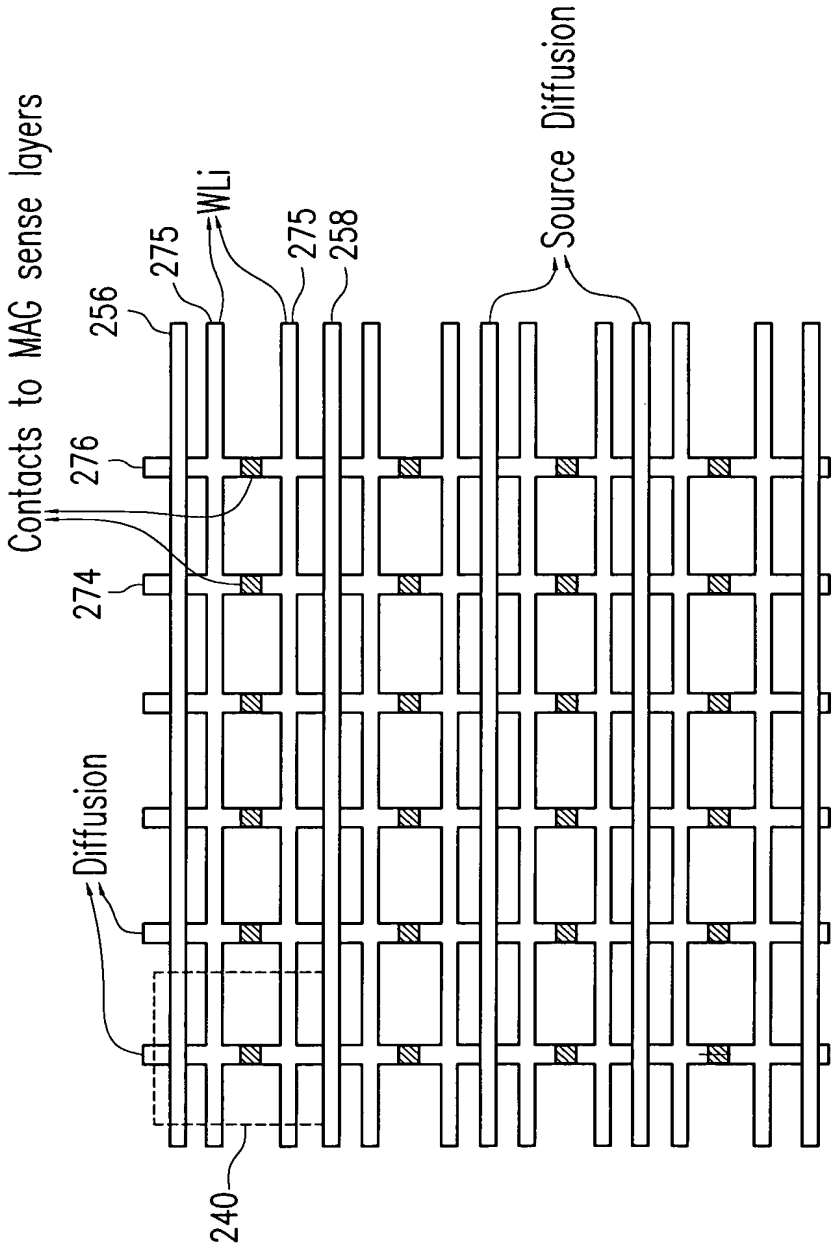
Contacts to MAG sense layers
276
274
Diffusion
240
256
275
WLi
275
258
Source Diffusion

FIG. 3B

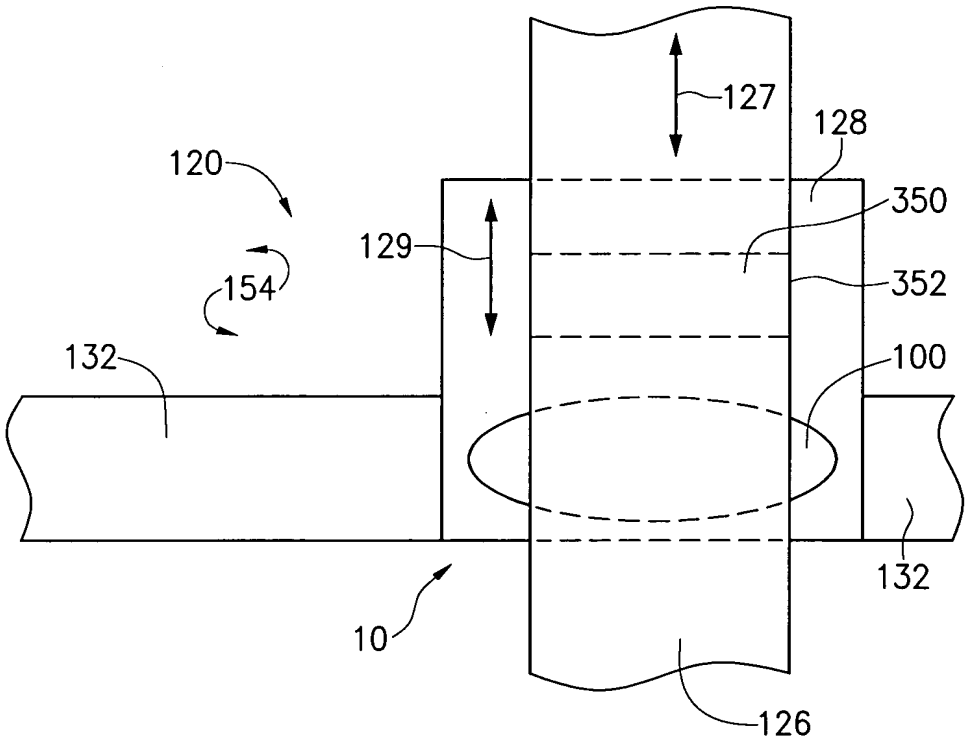

FIG. 4A

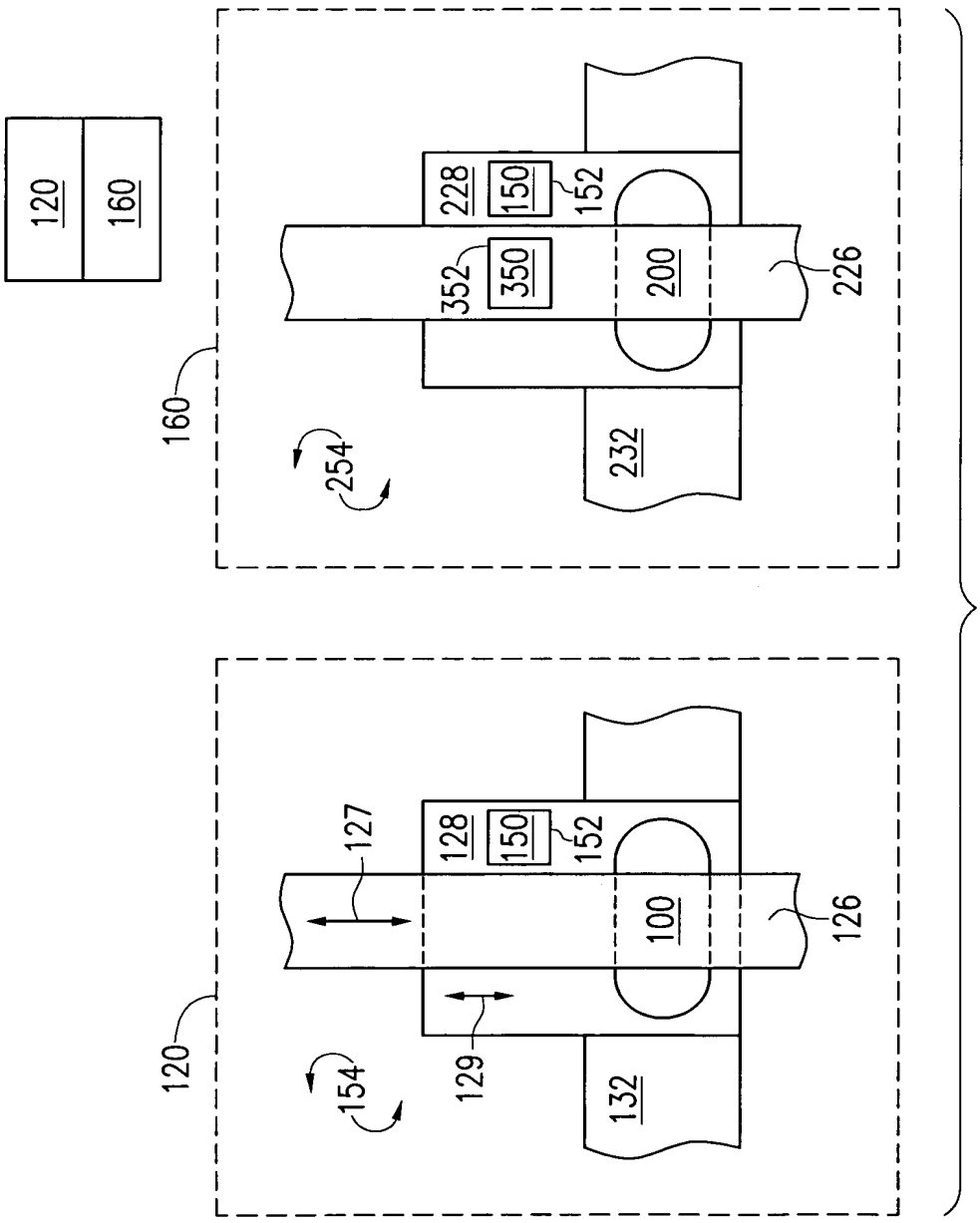
120
160
160
228
150
152
352
350
200
226
254
232
120
127
128
150
152
100
126
154
129
132

FIG. 4B

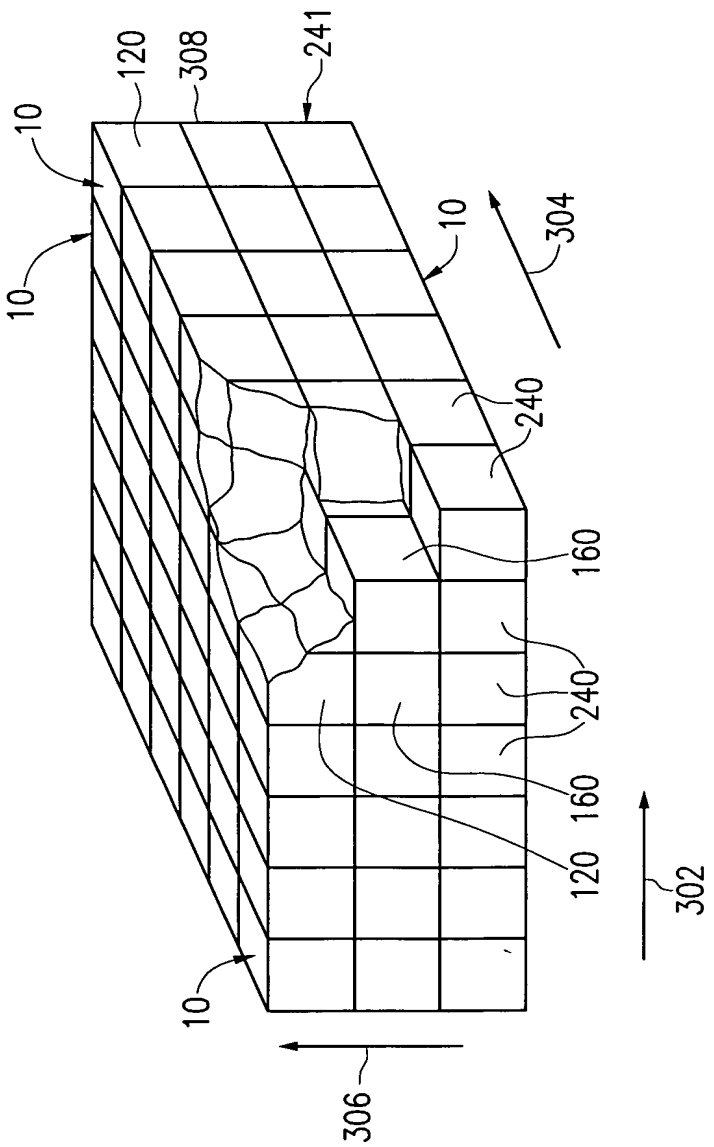

FIG. 5

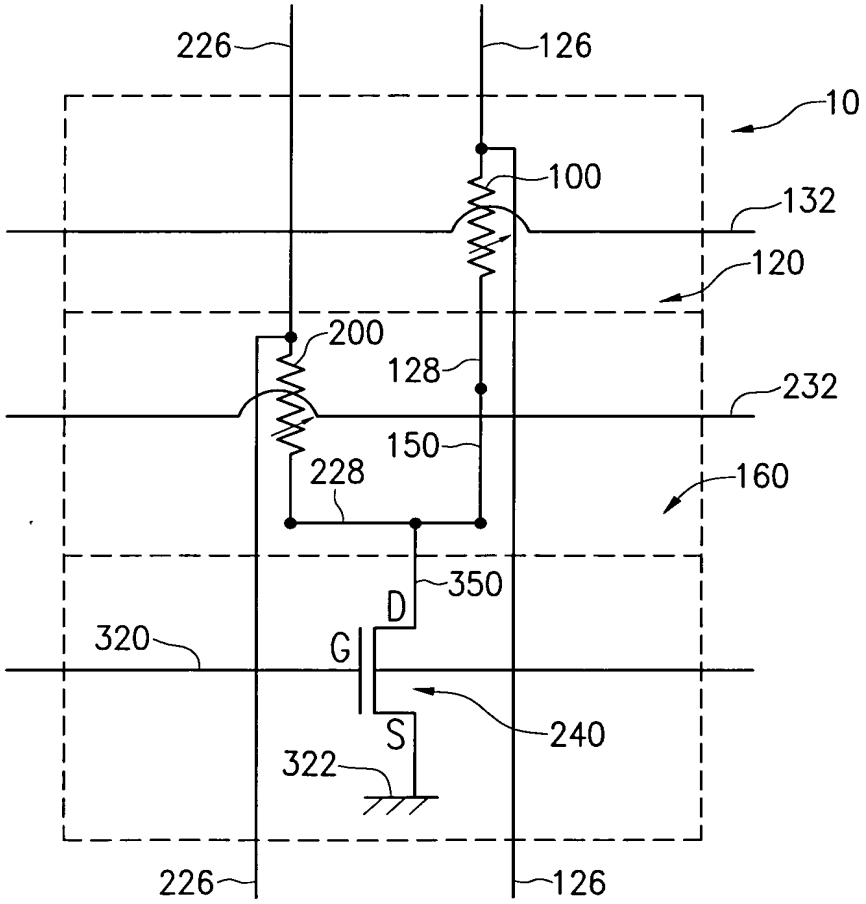
226
126
10
100
132
120
200
128
232
150
228
160
350
D
320
G
240
S
322
226
126

FIG. 6

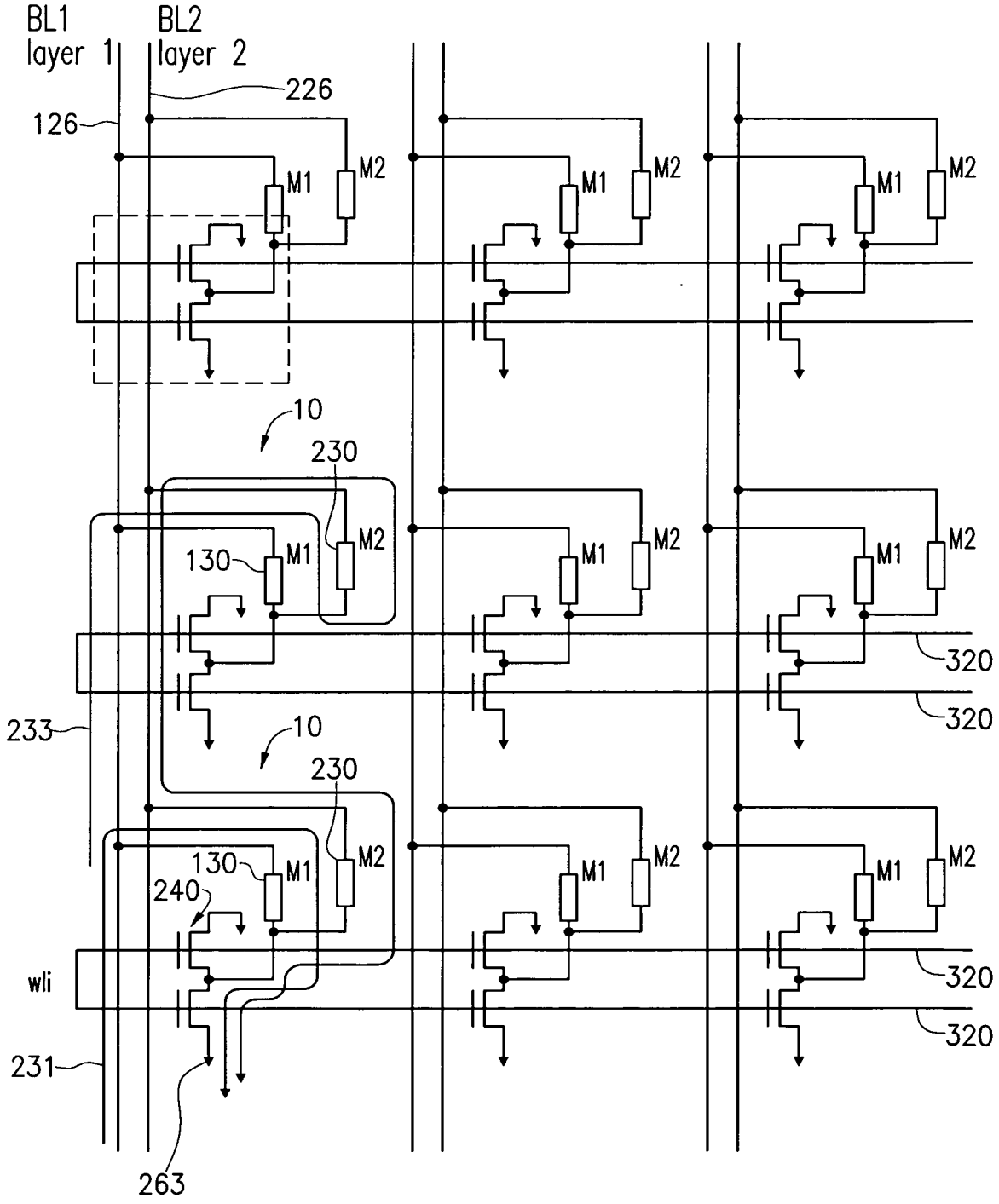
BL1
layer 1
BL2
layer 2
226
126
M1
M2
10
230
130
320
233
240
wli
231
263

FIG. 7

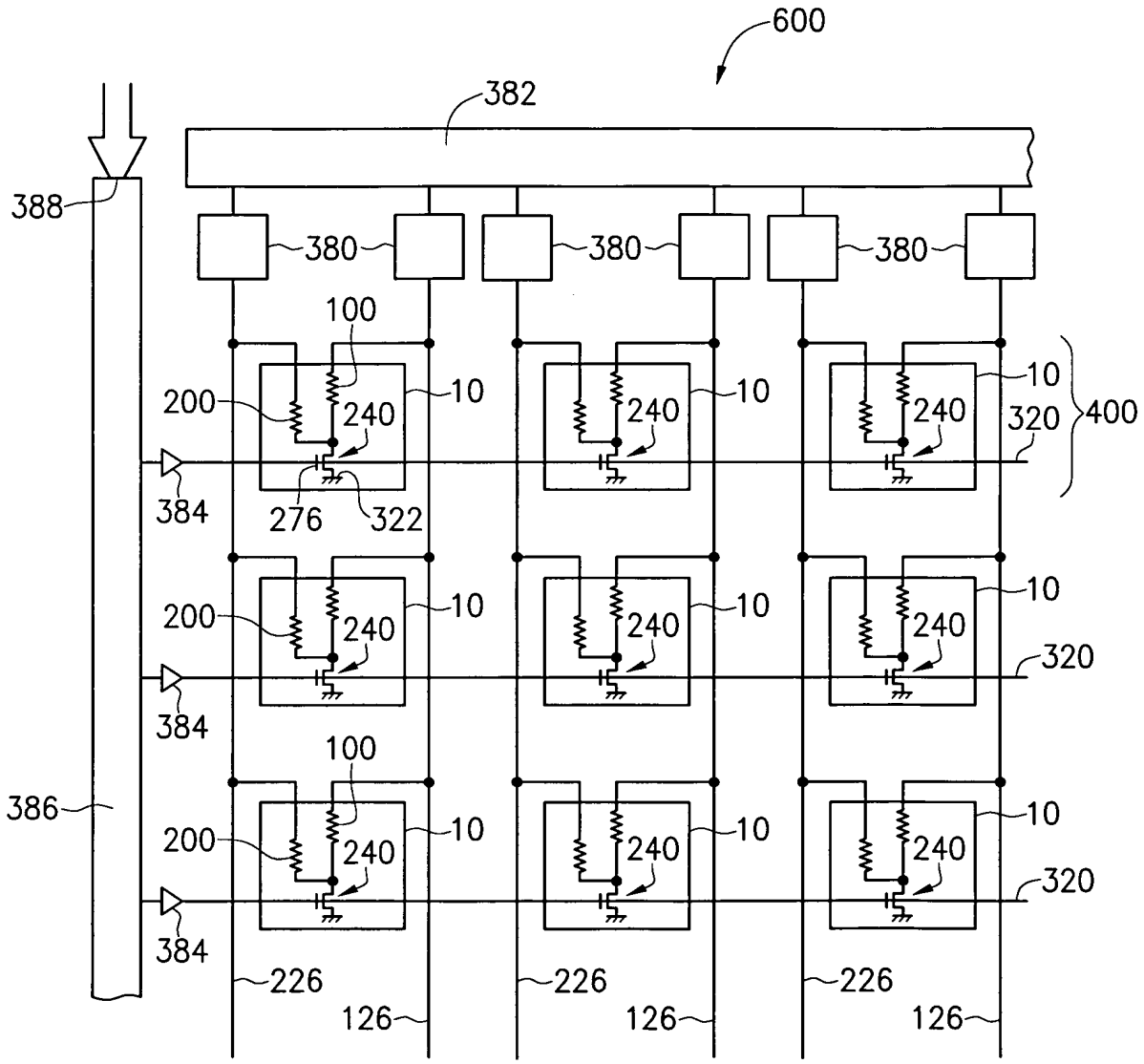
600
382
388
380
380
380
100
200
240
10
320
400
384
276
322
386
226
126

FIG. 8

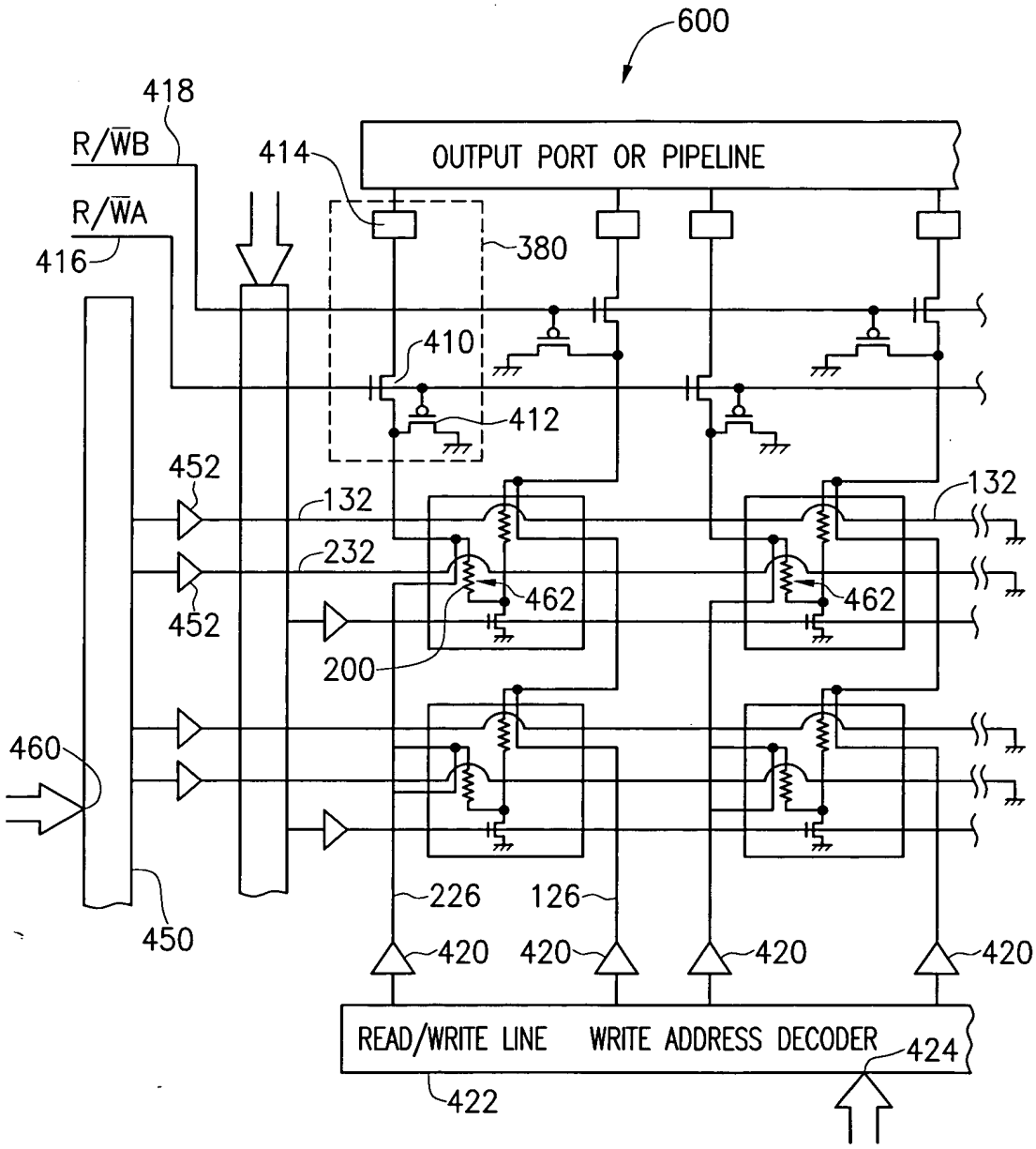
600
418
R/WB
414
OUTPUT PORT OR PIPELINE
R/WA
416
380
410
412
452
132
232
462
200
460
226
126
420
450
READ/WRITE LINE
WRITE ADDRESS DECODER
424
422

FIG. 9

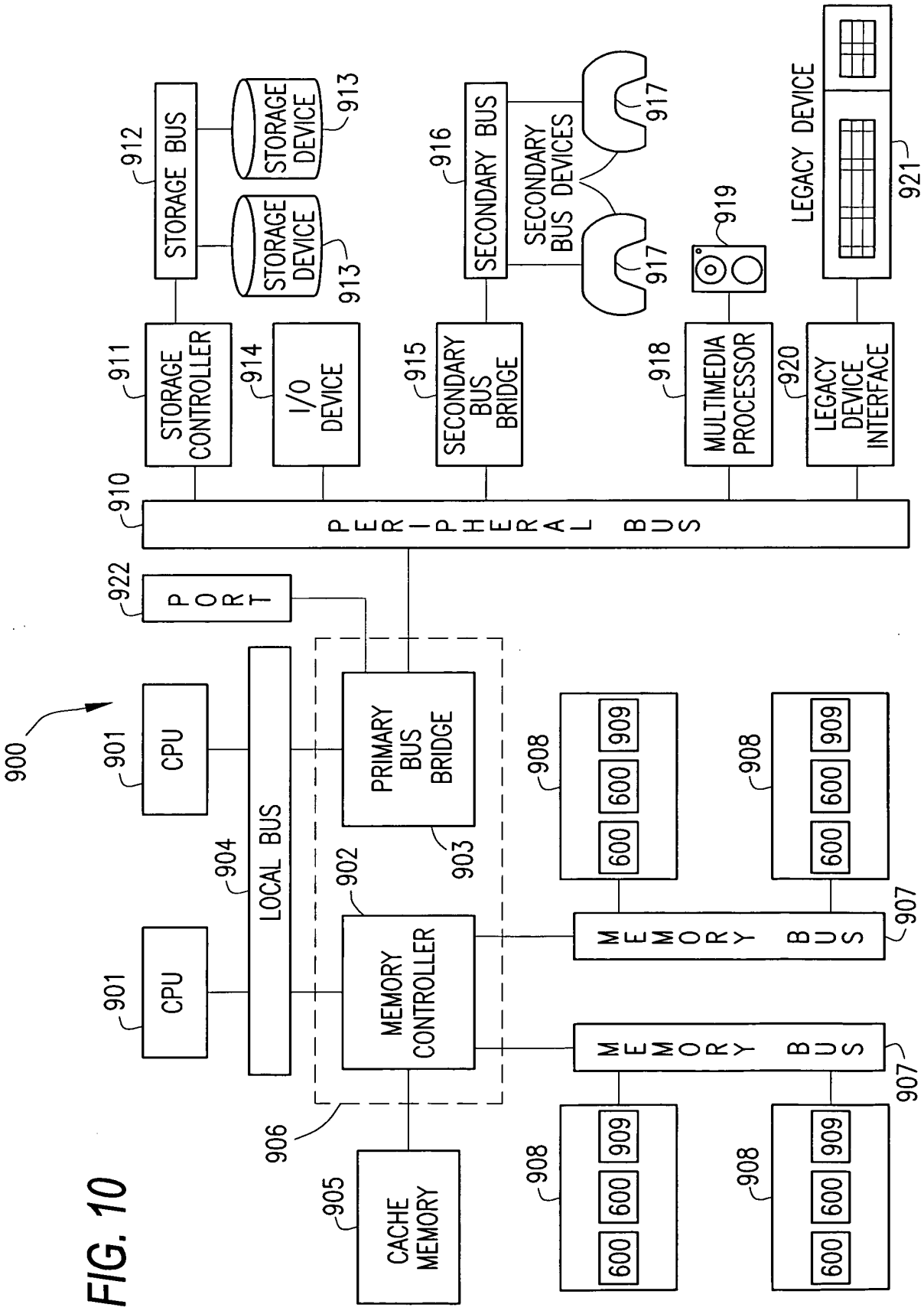
900
901
CPU
901
CPU
904
LOCAL BUS
902
MEMORY CONTROLLER
903
PRIMARY BUS BRIDGE
906
905
CACHE MEMORY
907
MEMORY BUS
907
MEMORY BUS
908
909
600
910
PERIPHERAL BUS
911
STORAGE CONTROLLER
912
STORAGE BUS
913
STORAGE DEVICE
913
STORAGE DEVICE
914
I/O DEVICE
915
SECONDARY BUS BRIDGE
916
SECONDARY BUS
917
SECONDARY BUS DEVICES
917
918
MULTIMEDIA PROCESSOR
919
920
LEGACY DEVICE INTERFACE
921
LEGACY DEVICE
922
PORT

FIG. 10